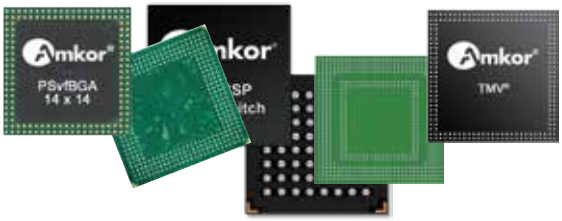
Data Sheet

Package on Package (PoP) Family



Bottom PoP Technologies

Amkor's popular Package Stackable Very Thin Fine Pitch BGA (PSvfBGA) platform supports single die, stacked die using wirebond or hybrid (FC plus wirebond) stacks and has been applied to Flip Chip (FC) applications to improve warpage control and package integrity through test and SMT handling.

As handheld microprocessors have transitioned to advanced CMOS nodes with higher speed cores with higher I/O, there has been a transition from wirebond to flip chip die designs. Flip chip enables the use of an exposed die bottom package that integrates the package stacking design features of PSvfBGA in a fcCSP assembly flow, which Amkor calls Package Stackable Flip Chip Chip Scale Package (PSfcCSP). PSfcCSP has a thin exposed FC die enabling fine pitch stacked interfaces at 0.5 mm pitch which is a challenge in a center molded PSvfBGA structure.

Continued development resulted in Amkor entering the second generation of PoP applications where new memory architectures, required in mobile multimedia applications, demand higher density stacked interfaces in combination with PoP mounted area and height reductions. The previous PSvfBGA and PSfcCSP structures limited the ability of the memory interface to scale in density and pitch, resulting in the need for a new bottom PoP structure.

Amkor developed new technologies to create the next generation PoP solution with interconnect vias through the mold cap. Known as Through Mold Via (TMV®), this technology provides a stable bottom package that enables use of thinner substrates with a larger die to package ratio. TMV enabled PoP can support single, stacked die or FC designs. TMV is an ideal solution for the emerging 0.4 mm pitch low power DDR2 memory interface requirements and enables the stacked interface to scale with solder ball pitch densities to 0.3 mm pitch or below.

The next few years promise to provide many new challenges and applications for PoP, as handheld multimedia applications continue to demand higher signal processing power and data storage capabilities. Amkor is committed to maintaining strong development and production capabilities to ensure we are at the forefront in meeting next generation PoP requirements.

Applications

PoP packages are designed for products requiring efficient memory architectures including multiple buses and increased memory density and performance, while reducing mounted area. Portable electronic products such as mobile phones (baseband or applications processor plus combo memory), digital cameras (image processor plus memory), PDAs, portable media players (audio/graphics processor plus memory), gaming and other mobile applications can benefit from the combination of stacked package and small footprint offered by Amkor's PoP family.

Visit Amkor Technology online for locations and to view the most current product information.

Features

- 10-15 mm body sizes tooled per product table, additional sizes based on demand
- Top package I/O interface 0.65 mm pitch accommodating 104 to 160 pin counts
- Wafer thinning/handling < 100 µm
- Mature PoP platform with consistent product performance and reliability
- Package configurations compliant with JEDEC standards
- Bottom PSvfBGA and top FBGA/Stacked CSP packages are well established in high volume production with multi-region and factory support
- Stacked package heights of 1.3 mm to 1.5 mm available in a variety of configurations (See Stack Up Tables on following pages)

Reliability Qualification

Amkor assures reliable performance by continuously monitoring key indices:

Package Level

• Moisture Resistance Testing	JEDEC Level 3 @ 260°C x 4 reflows
• Additional Test Data	30°C, 85% RH, 96 hours @ 260°C x 4
• HAST	130°C, 85% RH, 96 hours
• Temp/Humidity	85°C, 85% RH, 1000 hours
• Temp Cycle	-55°C/+125°C, 1000 cycles
• High Temp Storage	150°C, 1000 hours

Board Level

• Thermal Cycle	-40°C/+125°C, 1000 cycles

Package Dimensions

• PSvfBGA	10 x 10 mm to 15 x 15 mm
• PSfcCSP	12 x 12 mm to 13 x 13 mm
• TMV PoP	12 x 12 mm to 14 x 14 mm

Benefits as an Enabling Technology

PoP offers OEMs and EMS providers a flexible platform to cost effectively integrate logic plus memory devices in a 3D stacked architecture. Integration through PoP provides technical and business/logistics benefits:

- Greatly expands device and supplier options by simplifying the business logistics of stacking
- Integration controlled at the system level to best match stacked combinations including memory architecture with the system requirements
- JEDEC standards ensure broad component availability
- Improving time-to-market, inventory management and supply chain flexibility
- Eliminates margin stacking and expands technology reuse
- Provides the lowest total cost of ownership where complex 3D integration of logic plus memory is required

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Package on Package (PoP) Family

Process Highlights

- Die thickness 75 µm to 125 µm
- Bond pad pitch (min) 45 µm (in-line)
- Marking Laser
- Bump pitch (min) 200 & 300 mm wafers

Standard Materials

- Package Substrate
  - Conductor Copper
  - Dielectric Thin core FR5 or equivalent
- Die attach adhesive Conductive or non-conductive
- Encapsulant Epoxy mold compound
- Solder ball Pb-free
- Standard RoHS and green material sets available

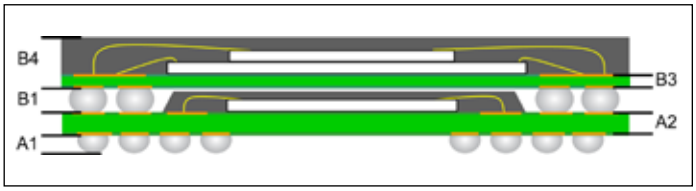
Test Services

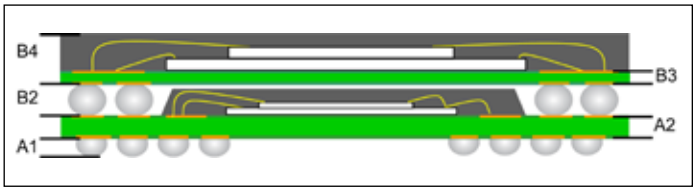
- Program generation/conversion
- Product engineering
- Dual sided contactor system available
- Tape and reel services

Shipping

- JEDEC trays

Cross-section PoP

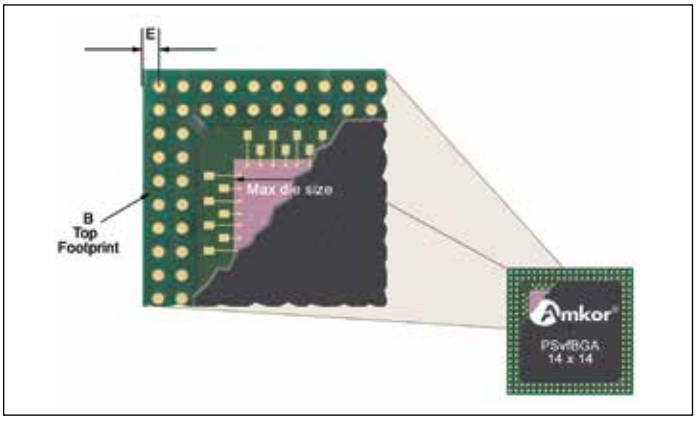


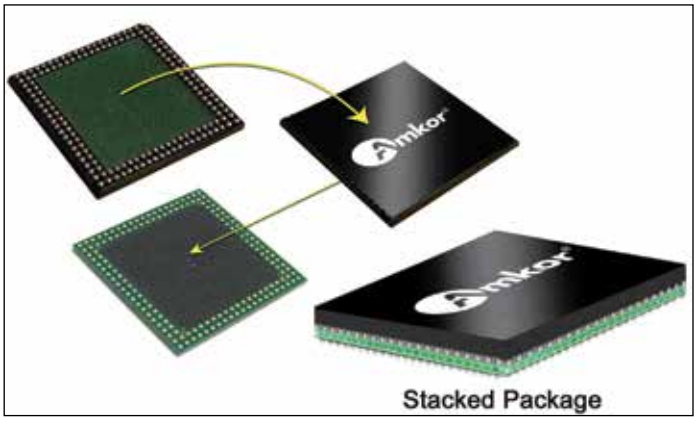


PoP Overall Stack Up Table (mm)

Symbol	FBGA + PSvfBGA		
	Min	Max	Nom
A1 (mounted, 0.5 pitch)	0.180	0.280	0.230
A2 (4L laminate)	0.260	0.340	0.300
B1 (stacked, 0.65 pitch), single die	0.270	0.330	0.300
B2 (stacked, 0.65 pitch), 2+0 die	0.320	0.380	0.350
B3 (2L laminate)	0.100	0.160	0.130
B4 (mold cap)	0.370	0.430	0.400
Overall Pkg Height	1.300	1.500	1.400

PSvfBGA Top View





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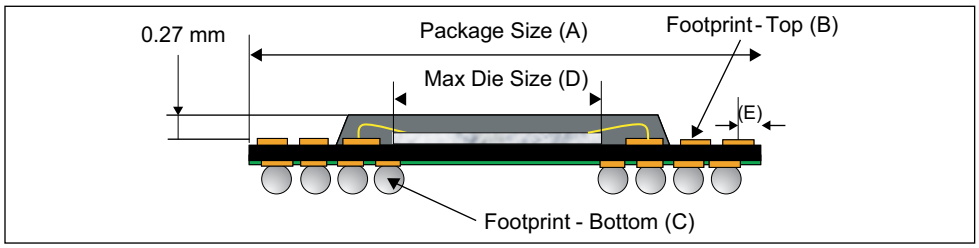
Data Sheet

Package on Package (PoP) Family

Cross-section PSvfBGA

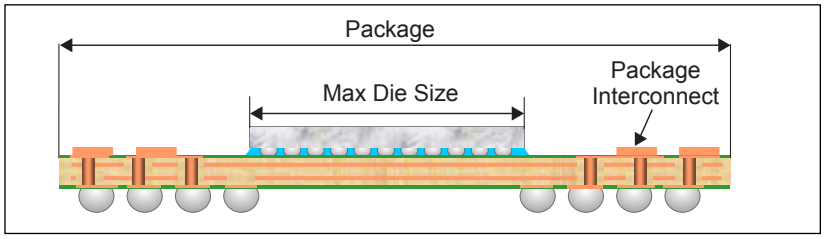


PSvfBGA Design Table for 0.65 mm Pitch 2 Row Stacked Interfaces

A	B		C	D	E	
Body Size (mm)	Package Interconnect		Bottom Package Ball Count Nom	Die Size (mm)	Package Interconnect Ball Center to Package Edge (mm)	Typical Wirecount for Given Package Size
	Matrix	Ball Count				
10	15	104	300	< 5.50	0.450	320
11	16	112	350	< 6.00	0.625	360
12	18	128	400	< 7.50	0.475	420
13	19	136	450	< 8.00	0.650	460
14	21	152	550	< 9.00	0.500	520
15	22	160	650	< 10.00	0.675	600

Dimensions are in line with JEDEC JC-11 standards for PoP packages in development
B - Based on 2 perimeter rows of interconnects at 0.65 mm pitch
C - Based on 4 perimeter rows of BGA balls to motherboard at 0.50 mm pitch

Cross-section PSfcCSP



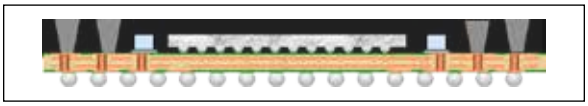
PSfcCSP Design Table for 0.5 mm Pitch 2 Row Stacked Interfaces

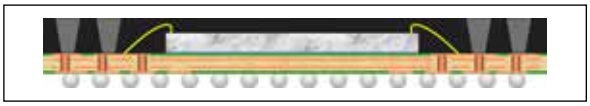
Body Size (mm)	Package Interconnect		Die Size (mm)
	Matrix	Ball Count	
10	19	136	<6.00
11	21	152	<7.00
12	23	168	<8.00
13	25	184	<9.00
14	27	200	<9.50
15	29	216	<10.00

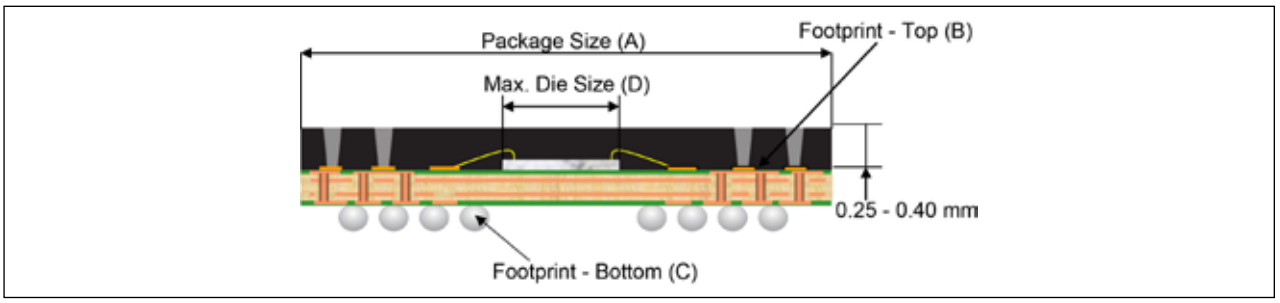
Data Sheet

Package on Package (PoP) Family

Cross-sections TMV® PoP

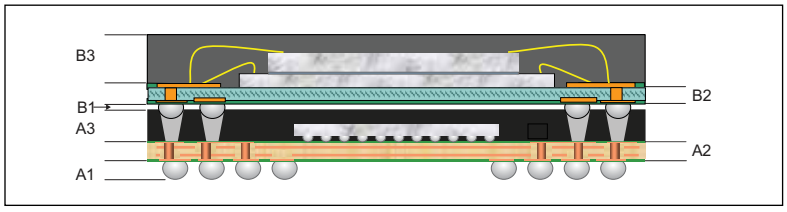






TMV® Design Table for 0.4 mm Pitch 2 Row Stacked Interfaces

A	B		C	D	E
Body Size (mm)	Package Interconnect - 2 Rows		Bottom Ball Count 0.4 mm Pitch (Full Matrix)	Max Die Size Flip Chip (mm)	Max Die Size Wirebond (mm)
	Matrix	Top Ball Count			
10	23	168	529	7.00	6.00
11	26	192	676	8.00	7.00
12	28	208	784	9.00	8.00
13	31	232	961	10.00	9.00



TMV® PoP Overall Stack Up Table (mm)

Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L laminate)	0.220	0.300	0.260
A3 (Mold cap)	0.230	0.280	0.250
B1 (Stacked gap)	0.020	0.080	0.050
B2 (2L laminate)	0.100	0.160	0.130
B3 (Mold cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

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DS586G
Rev Date: 12/12

Technology Solutions

System in Package (SiP)

Semiconductor industry demands for higher levels of integration and lower costs coupled with a growing awareness of complete system configuration have continued to drive the popularity of System in Package (SiP) solutions. Amkor's SiP technology is an ideal solution in markets that demand smaller size with increased functionality. With more than 1 billion SiP devices assembled and tested over more than 10 years, Amkor Technology has a proven track record as the industry leader in SiP assembly technology. Contact us today and let us add you to our growing list of customers who have been successful with System in Package technology.

What is System in Package?

System-in-Package (SiP) is more than just an IC package containing multiple die. Amkor defines SiP as: System in Package is characterized by any combination of one or more Integrated Circuit(s) of different functionalities, which may include passive components and/or MEMS assembled into a single package that performs as a system or sub-system. SiP may contain one or more IC chips (either wirebonded,flip chip, or both) plus other components that are traditionally found on the system mother board such as:

- Surface mount discrete passive (any common format including 01005 size)
- Integrated passive networks (IPN)
- Integrated passive devices (IPD, either glass or Si type)
- Passives embedded inside or patterned on the substrate
- Die embedded in the package substrate
- SAW/BAW filters
- EMI shields
- Pre-packaged ICs
- Connectors
- Mechanical parts

The power of SiP is the ability to bring together many IC and package assembly and test technologies to create highly integrated products with optimized cost, size and performance.

Total System in Package Solutions

In an SiP approach, one must consider not only the traditional elements of package assembly, but also design aspects relating to the overall system functional requirements and manufacturing process, as well as supply chain management and test.

System design becomes paramount to the overall success of developing a System in Package. Early in the overall system design, the customer and Amkor discuss and agree upon all elements of the system requirements to ensure success of the design. With this in mind, Amkor has significantly expanded our design capability to combine traditional layout expertise with digital and RF circuit design and system modeling. Amkor can also translate your reference designs for use in SiP development. Working closely with the customer, Amkor can model circuits electrically, mechanically and thermally, which will reduce design iterations and minimize time-to-market.

After modeling, Amkor can prototype the package using production-capable equipment to ensure ease of transfer into one of our high volume factory sites. Supply chain considerations play a major factor in the success of SiP product realization and impact both design and manufacturing. Amkor has expanded its traditional supply chain expertise into passive components, and other parts not traditionally found in the package assembly environment. Amkor can manage the supply chain to ensure successful SiP development and production.

Thermal Solutions for SiP

Inevitably, higher levels of integration result in thermal challenges. As part of our co-design service, we capture not only electrical but also thermal constraints early on so that the package solution will meet all your performance criteria. Amkor has a menu of thermal enhancement options to ensure that your die runs cool and we can deploy any of the following for your device:

1. Thermal vias
2. Stacked Cu-filled via structures
3. Thermal “breadloaf” structures using coreless laminate
4. Direct-to-metal die attach pad structure
5. Enhanced thermal die attach compound
6. Enhanced thermal mold compound
7. Molded-in heatspreaders

As part of our co-design service we will help you identify the optimum and most cost-competitive thermal enhancements that your device requires to satisfy your customer’s operating conditions and field life expectations.

System in Package (SiP)

Markets for System in Package

Existing market uses for SiP include RF and wireless devices (such as power amplifiers, GPS/ GNSS modules, cellular handset and cellular infrastructure, Bluetooth® solutions), Netbooks, digital baseband solutions for the wireless markets and controllers for hard drives in the storage market, and automotive applications including under-hood ECU, sensory modules and infotainment.

SiP technology can also be used to enhance single component packages that require improved circuit performance and reduced board real estate. System in Package technology allows multiple advanced packaging technologies to be combined to create solutions customized to each end application.

Amkor is heavily involved in providing SiP solutions for RF and wireless applications such as digital cellular, Bluetooth®, 802.11 modems and GPS. We have RF design engineers on staff to assist customers in designing RF SiPs, including creating circuit elements (e.g., baluns and filters) in the substrate which may eliminate discrete components. Amkor is able to meet all design, material and manufacturing requirements for RF SiPs, including such items as wire length control and substrate materials (LTCC, laminate and others). We have successfully used our RF design and packaging capability to integrate shields and antennas directly into the SiP.

Amkor has developed expertise in RF testing including test system software/hardware development and manufacturing test. We have an internally-developed, world class test platform that typically offers a 50% to 80% reduction in test time for common RF parts -- PAs, LNAs, and combinations in Integrated Front Ends (IFE).

System in Package Benefits

As with System on Chip (SoC), Amkor's SiP technology is an ideal solution in markets that demand smaller size with increased functionality. However, SiP has the added benefit of compatibility with die design changes and integration of various die technologies (e.g., Si, GaAs, SiGe, SOI, MEMS) without the high cost and lead time associated with SoC development and manufacturing. Amkor Technology has leveraged its single chip assembly and test technology into SiP development.

Additional Benefits of s System in Package Approach

- Smaller size solution than individually-packaged ICs
- Higher performance through shorter interconnect paths, better dimensional tolerances and local shielding
- Lower overall cost of ownership
  - Eliminate packaging (multiple ICs now in one package)
  - Reduces system board complexity and layer count by moving to the SiP
  - Uses less system board space than individually packaged ICs
  - Reduced overhead for the customer (Amkor offers turnkey solutions for assembly, test, supply chain management and value-added services)
  - Known good modules
- Reduced time to market - The modules and main system assembly can be developed concurrently
  - Changes can be made to the SiP without costly changes to the system board
  - Design flexibility and easy redesign versus complex System on Chip design
  - SiP allows plug-and-play insertion into one or multiple systems
- With proper consideration to design, Amkor's SiP packages are able to meet JEDEC L3/260 moisture resistance and are passing Amkor's internal SQLb.

System in Package is the modular design approach offering unprecedented flexibility in product development. The end user benefits from a faster time-to-market, reduced cycle times for system design, lower development risk as compared to SoC IC development, flexibility, tuned functional performance, and in the end, a lower overall cost of ownership

System in Package (SiP)

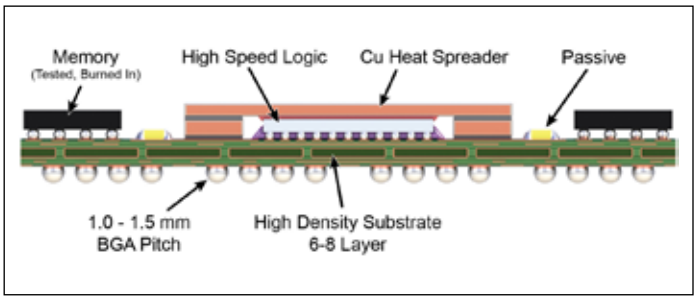
Global Manufacturing Footprint for SiP

Amkor has a very broad global footprint for assembly and test, and offers SiP capability at each of our main factories. Our primary centers for mass production are in the Philippines (P3) and Korea (K4) but SiP packaging can be supported at additional locations. Amkor SIP factories are equipped with the latest generation surface mount equipment to provide these attributes:

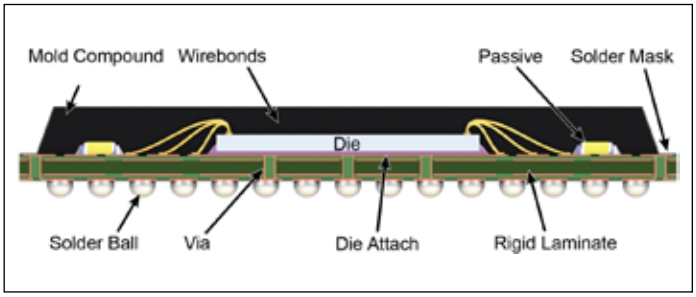
1. Ultra high-speed SMT placement machines which have leading-edge component placement accuracy – best quality and lowest cost.
2. Flexible placement machines which are better suited for odd-form component placement
3. Capable of placing any common component format available in tape and reel format down to and including the smallest 01005 size.
4. Capable of mounting bumped die directly from wafer tape
5. Solder paste stencil printing, flux stencil printing, flux jetting or flux dipping are all supported processes.
6. 100% inline solder paste automatic optical inspection is available
7. All common RoHS/Green compliant solder alloys are supported

Amkor supports SiP production in many different package formats including both laminate and leadframe molded array format along with PBGA, and capturing both wire bond or flip chip first level connectivity. In addition, Amkor supports a wide variety of custom packages such as daughter cards, fingerprint sensors, etc.

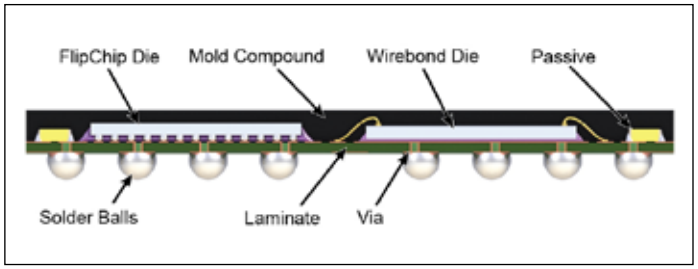
Cross-section SuperFC™ SiP



Cross-section SiP-PBGA



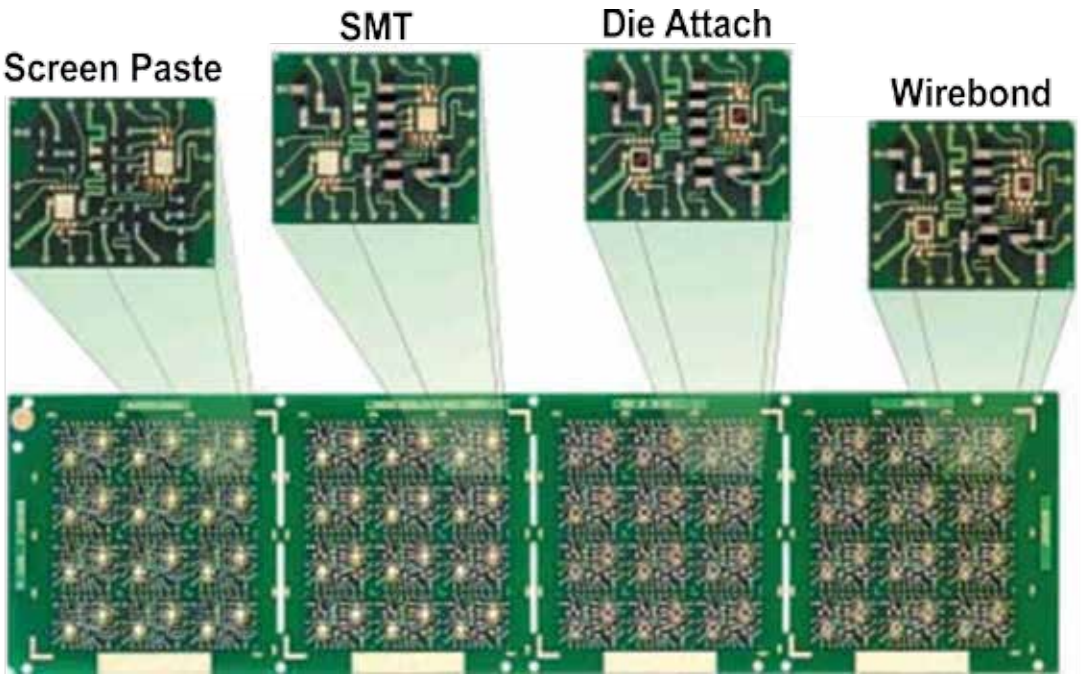
Cross-section SiP-CABGA



Technology Solutions

System in Package (SiP)

System in Package Manufacturing Sequence



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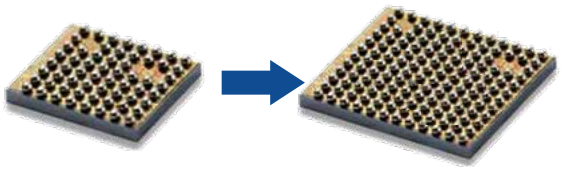
TS101M
Rev Date: 5/14

WLCSP

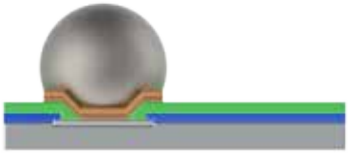


Wafer Level Processing & Die Processing Services (WLP/DPS)

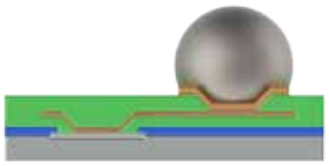
Amkor offers Wafer Level Chip Scale Packaging (WLCSP) providing a solder interconnection directly between your device and your end product's motherboard. WLCSP includes wafer bumping (with or without pad layer redistiribution or RDL), wafer level final test, device singulation and packing in tape & reel to support a full turn-key solution. Amkor's robust Under Bump Metallurgy (UBM) over PBO or PI dielectric layers on the die active surface providing a reliable interconnect solution able to survive harsh board level conditions meeting the demands of the growing global consumer market place for portable electronics.

Fueling Growth

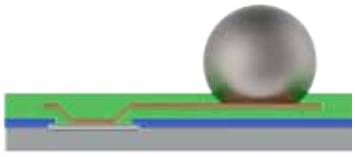
- Small packages in mobile critical to maximize battery size
- Level of adoption in fastest growing markets (i.e., tablets and smartphones)
- Dis-integration of high performance functions from processors to new specialized devices(e.g., audio)
- Fewer cycles through electrical test
- Lower cost to EMS assembly MSL L1 package from T&R
- Improved SMT-compatible underfill processes at EMS companies increase prior die size limits



The **CSP^{nl} Bump on Repassivation (BoR)** option provides a reliable, cost-effective, true chip-size package on devices not requiring redistribution. The BoR option utilizes a repassivation polymer layer with excellent electrical/mechanical properties. A UBM is added, and solder bumps are then placed directly over die I/O pads. CSPnl is designed to utilize industry-standard surface mount assembly and reflow techniques.



The **CSP^{nl} Bump on Redistribution** option adds a plated copper Redistribution Layer (RDL) to route I/O pads to JEDEC/EIAJ standard pitches, avoiding the need to redesign legacy parts for CSP applications. A nickel-based or thick copper UBM offerings, along with polyimide or PBO dielectrics, provide best in class board level reliability performance. CSPnl with RDL utilizes industry-standard surface mount assembly and reflow techniques, and does not require underfill on qualified device size and I/O layouts.



The **CSP^{n3}** option utilizes one layer of copper for both redistribution and UBM. This simplified process flow reduces cost and cycle time by over 20%. CSPn3 has been in production since 2009 and as of 2012 is at a run rate of over 1 billion units annualized.

Applications

The WLCSP package family is applicable for a wide range of semiconductor device types from high end RF WLAN combo chips, to FPGAs, power management, Flash/EEPROM, integrated passive networks and standard analog. WLCSP offers the lowest total cost of ownership enabling higher semiconductor content while leveraging the smallest form factor and one of the highest performing, most reliable, semiconductor package platforms on the market today. WLCSP is ideally suited for, but not limited to, mobile phones, tablets, netbook PCs, disk drives, digital still & video cameras, navigation devices, game controllers, other portable/remote products and some automotive end applications.

Wafer Level Features

- 4-196 ball count
- Small body 0.64 mm^2 to large 50.0 mm^2 body size
- PBO & Polyimide (PI) Repassivation and Redistribution Layer (RDL) available
- Electroplated Sn/Ag < 0.3 µm and SAC Alloy ball-loaded bumping options ≥ 0.3 µm pitch
- Reliable thick Cu UBM or Ni/Au for best in class EM performance
- Compatible with conventional SMT assembly and test techniques

Die Level Features

- Best in class component and board level reliability
- JEDEC tested board level performance demonstrated without underfill
- Precision edge quality ensuring device integrity at board mount
- Back-side laminate coating available
- Cost effective T&R packaging solutions for small ICs
- Ultra-thin backgrinding for embedded die applications
- Full turnkey WLP, contact probe and DPS supported in Taiwan, China and Korea
- Wide selection of pocket tape carrier options

Visit Amkor Technology online for locations and to view the most current product information.

DS720F
Rev Date: 2/13

WLCSP

Package Options

Ball Loading	Pitch	Sphere Diameter
	0.50 mm	0.30 mm
	0.40 mm	0.25 mm
	0.30 mm	0.20 mm

Reliability Qualification

Package Level:

- Preconditioning at Level 1 (Unlimited out of bag life) — 85°C/85% RH, 168 hours, reflow @ 260°C peak
- Temp Cycle — -55°C/+125°C, 1000 cycles
- High Temp Storage — 150°C, 1000 hours

Board Level:

- Temp Cycle — -40°C/+125°C, 15 min. ramp rate, ≥ 500 cycles
- Drop Test — JEDEC condition B (1500G), ≥ 100 drops

Process Highlights

- Die thickness — 225 µm* to 450 µm
- Bump height — 0.5 mm Pitch: 250 µm
0.4 mm Pitch: 210 µm
0.3 mm Pitch: 170 µm
- Solder ball pitch (ball loaded)
Pitch (plated) — 0.28, 0.3, 0.35, 0.4, 0.5 mm
0.12 to 0.25 mm
- Solder sphere diameter — 0.2, 0.25, 0.3 mm
- Redistribution trace/space (min) — CSPnl: 12/12 µm
CSPn3: 15/15 µm
- Via diameter (min) — PBO: 15 µm
Polyimide: 35 µm
- Backside laminate (black) — Available
- Saw street (min) — 65 µm (passivation free space)

Standard Materials

- Dielectric materials — PBO and polyimide
- RDL metalization — Plated copper
- UBM — Thick Cu or Ni-based
- Solder composition (ball loaded)
(plated) — Pb-free SAC alloys
Sn/Ag Pb-free, Cu pillar

Shipping

Carrier tape — 7″, 13″ reels

*Advanced manufacturing rules may be required. Contact Amkor Business Unit for additional information.

Capabilities and Services

WLP

- Design services available
  - Layout
  - Mask tooling
- Wafer RDL patterning and bumping (ball sphere loaded or plated)
- Automated Optical Inspection (AOI) for best in class quality assurance
- Wafer map generation

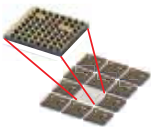
Inspect & Clean
PBO or PI 1
RDL Seed Deposition
Resist Processing
Cu RDL Plating
Resist & Seed Removal
PBO or PI 2
UBM Seed Deposition
Resist Processing
Cu or Ni-based UBM
Resist & Seed Removal
Ball Place

Test

Contact Probe

- Test software and hardware development
- Probe card design, service and support
- Test program transfer
- Wafer sort for RF, memory, logic and analog applications

DPS



Backgrind
Backside Lamination
Laser Mark
Singulation
Tape & Reel
AOI

- Best in class singulated device edge quality for all Si nodes
- Shipping material design and supply management
- Drop ship to final customer available

Visit Amkor Technology online for locations and to view the most current product information.

Amkor Technology®

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